In the claims:

1. (Currently amended) A dielectric substrate having a multiturn inductor comprising:

a) a multilayer dielectric body comprising a plurality of layers;

b) a multiturn inductor buried within the dielectric body, each turn of the inductor comprising a bottom portion, a top portion and two side portions, the bottom portion and top portion being parallel and in different layers of the dielectric body, the side portions being parallel to each other and extending between the top and bottom portions and comprising vias in the dielectric body, wherein the top and bottom portions have a lower crossectional area than the side portions and wherein the top and bottom portions each comprise two parallel wiring lines in juxtaposition.

2. (Previously presented) The dielectric substrate of claim 1 wherein the top and bottom portions comprise wiring lines situated in respective layers of the dielectric body.

Claim 3. (Canceled)

4. (Currently amended) The dielectric substrate of claim 1 ~~3~~ further comprising vias connecting the parallel wiring lines of each of the top and bottom portions.

5. (Previously presented) The dielectric substrate of claim 4 wherein the parallel wiring lines have ends and wherein the vias connecting the parallel wiring lines are only at the ends of the lines.

6. (Previously presented) The dielectric substrate of claim 4 wherein the parallel wiring lines each have a length and wherein the vias connecting the parallel wiring lines are spaced along the length of the parallel wiring lines.

7. (Original) The dielectric substrate of claim 1 wherein the turns of the multiturn inductor form a toroidal shape.

8. (Previously presented) The dielectric substrate of claim 1 wherein the multiturn inductor is tuned by tapping the multiturn inductor at selected locations.

9. (Previously presented) The dielectric substrate of claim 8 further comprising deletion of a portion of the multiturn inductor so as to tune the multiturn inductor.

10. (Previously presented) The dielectric substrate of claim 1 wherein the multiturn inductor is tuned by the addition of at least one additional buried loop to the multiturn inductor.

11. (Previously presented) The dielectric substrate of claim 1 wherein the multiturn inductor is tuned by the addition of a plate adjacent to the multiturn inductor, the plate being electrically isolated from the multiturn inductor.

12. (Previously presented) The dielectric substrate of claim 1 wherein the multiturn inductor is tuned by the addition of a plate adjacent to the multiturn inductor, the plate being electrically connected to the multiturn inductor.

13. (Original) The dielectric substrate of claim 1 wherein the multiturn inductor is a first multiturn inductor and further comprising a second buried multiturn inductor near the first multiturn inductor but electrically isolated therefrom, the first and second multiturn inductors cooperating to form a transformer.

Claims 14 to 20 (Canceled).

21. (Previously presented) The dielectric substrate of claim 1 wherein the top and bottom portions are planar in shape so as to comprise a flat portion having a width and a thickness less than the width, the side portions having a circular contact surface and the flat portion of the top and bottom portions in contact with the circular contact surface of the side portion.

22. (Previously presented) The dielectric substrate of claim 1 wherein the top and bottom portions are planar wiring lines and the side portions are vias having a circular contact surface wherein the planar wiring lines directly contact the circular contact surface of the vias.

23. (Currently amended) A dielectric substrate having a multiturn inductor comprising:

a) a multilayer dielectric body comprising a plurality of layers;

b) a multiturn inductor buried within the dielectric body, each turn of the inductor comprising a bottom portion, a top portion and two side portions, the bottom portion and top portion being parallel and in different layers of the dielectric body, the side portions being parallel to each other and extending between the top and bottom portions and comprising vias in the dielectric body, wherein the top and bottom portions have a lower crossectional area than the side portions and ~~The dielectric substrate of claim 1~~ wherein the top and bottom portions each comprise at least two parallel wiring lines of unequal length in juxtaposition.